

Atty D cket No.: JCLA7737

Serial No.: 10/015,414

**REMARKS****Present Status of the Application**

It is noted with a great appreciation that the Examiner allowed claim 8. Claims 5-8 remain pending of which claim 5 has been amended to more explicitly and precisely describe the claimed invention. It is believed that no new matters adds by way the amendments made to claims or otherwise to the application. For at least the following reasons, Applicants respectfully submit that claims 5-8 are in proper condition for allowance. Reconsideration is respectfully requested.

**Discussion of claim rejections**

The Office Action rejected claims 5-7 under 35 U.S.C. 103(a) as being unpatentable over Bergemont et al. (US-6,327,187, hereinafter Bergemont).

Applicants respectfully disagree and traverse the above rejections as follows. Independent claim 5 is allowable for at least the reason that substantially Bergemont fail to teach, suggest or disclose every features of the claimed invention. More specifically, Bergemont fail to teach, suggest or disclose a memory cell comprising a nitride tunneling layer. Instead, substantially Bergemont teaches an ONO gate oxide structure which is similar to the conventional art. Therefore it is clear that Bergemont teaches forming an oxide tunneling layer. Accordingly, Applicants respectfully submit that Bergemont teaches away from the claimed invention in this regard.

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Further, the method of erasing a non-volatile memory cell comprises: "applying a first positive bias to the drain region, applying a second positive bias to the gate conductive layer, and grounding the source region and the substrate to generate hot electron/holes in a channel region, wherein the hot electron/holes are injected into the charge-trapping layer through the nitride tunneling layer, as required by claim 5. The advantage of using the nitride tunneling layer that is disposed between the substrate and the charge trapping layer is that the energy barrier for an electron and electron hole can be effectively lowered compared to that of using oxide tunneling layer so that hot channel carrier injection can be effectively promoted, and therefore the operating speed of the memory device can be effectively increased. Because Bergemont substantially teaches using an oxide tunneling layer instead of a nitride tunneling layer, therefore, it is clear that Bergemont fails to teach using the nitride tunneling layer and therefore cannot possibly render the use of nitride tunneling layer obvious, much less teaching regarding the advantages of using the nitride tunneling layer.

For at least the forgoing reason, claims 5-7 patently define over Bergemont. Reconsideration and withdrawal of these rejections is respectfully requested.

SOWOS  
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SiO<sub>2</sub> NiO<sub>2</sub>

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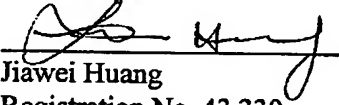
**CONCLUSION**

For at least the foregoing reasons, it is believed that all pending claims 5-8 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

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